Utilizing FPGA as Synthetic Instruments for Test Reuse

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Problems to solve (in field test)

- ATS obsolescence with rapidly advancing technologies
  - Speed, bus protocol, etc.
  - Handshaking, non-determinism
- Legacy ATS to deal with thousands of UUT types
  - Service depot limitations (space, legacies)
  - Very few units, but high diversity of units
- Development cost of new ATE hardware/software and TPS
  - Custom circuits require longer development time for new ATE
  - New ATE requires total rewrite of ***ALL*** test program and test interfaces

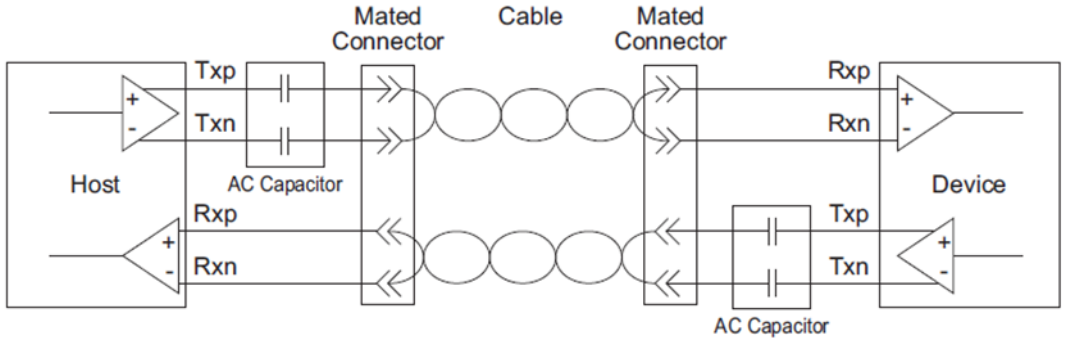
A very different situation as compared to Manufacturing Test !

HSIO Test Challenges

High data rate

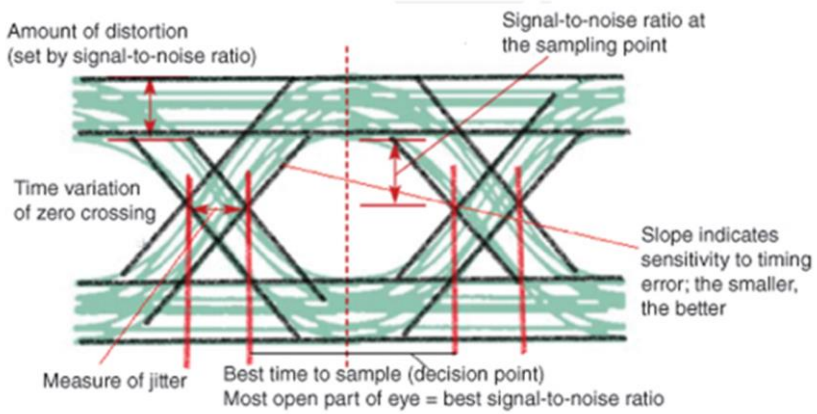
8B/10B encoding

Clocking embedding



differential

Low voltage swing

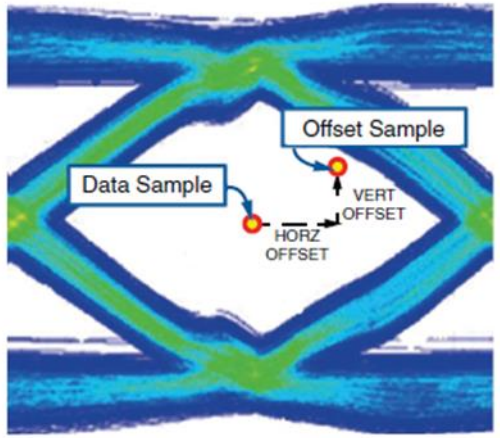


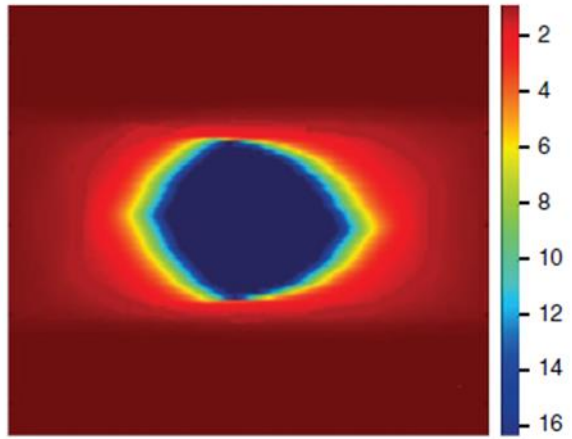
Channel loss

De-emphasis

Pre-emphasis

Equalization



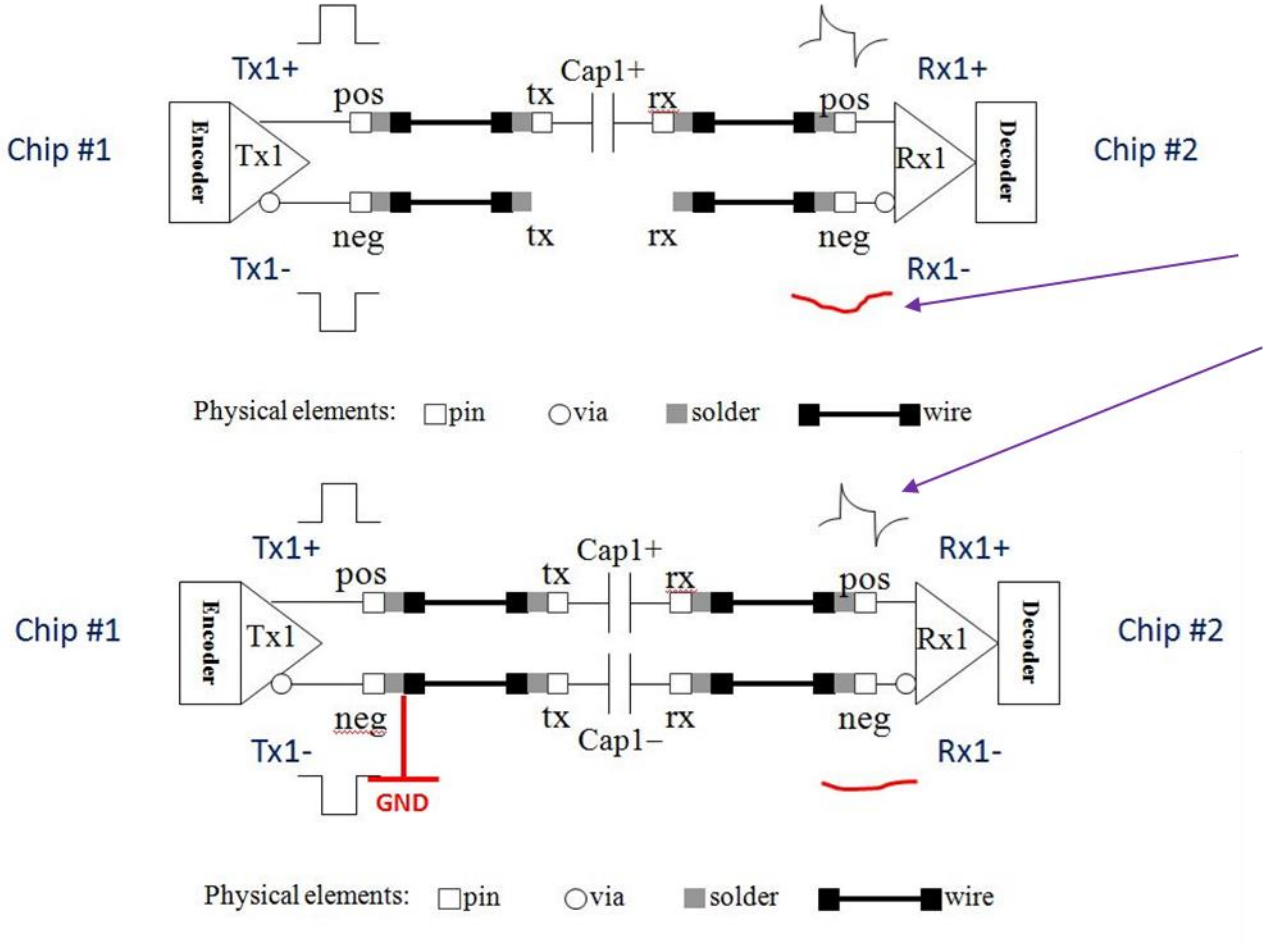


BER EYE DIAGRAM

ERROR RETRY

Handshaking initialization

Sometimes, getting the right answer may not be right



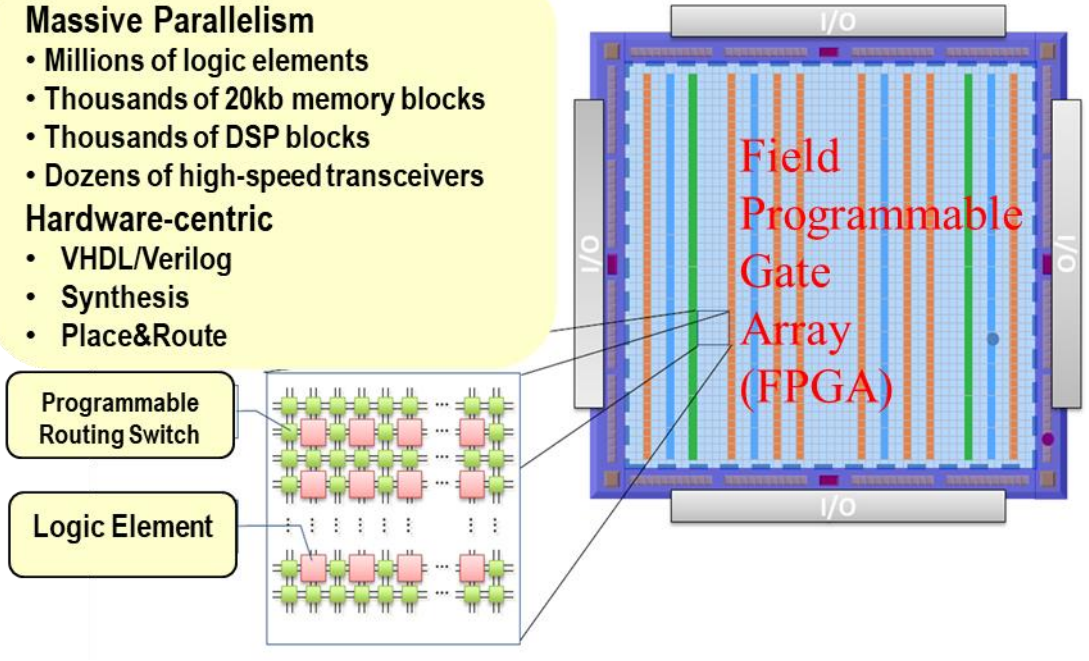
Despite having open/shorts, data may still be captured due to differential nature of signaling

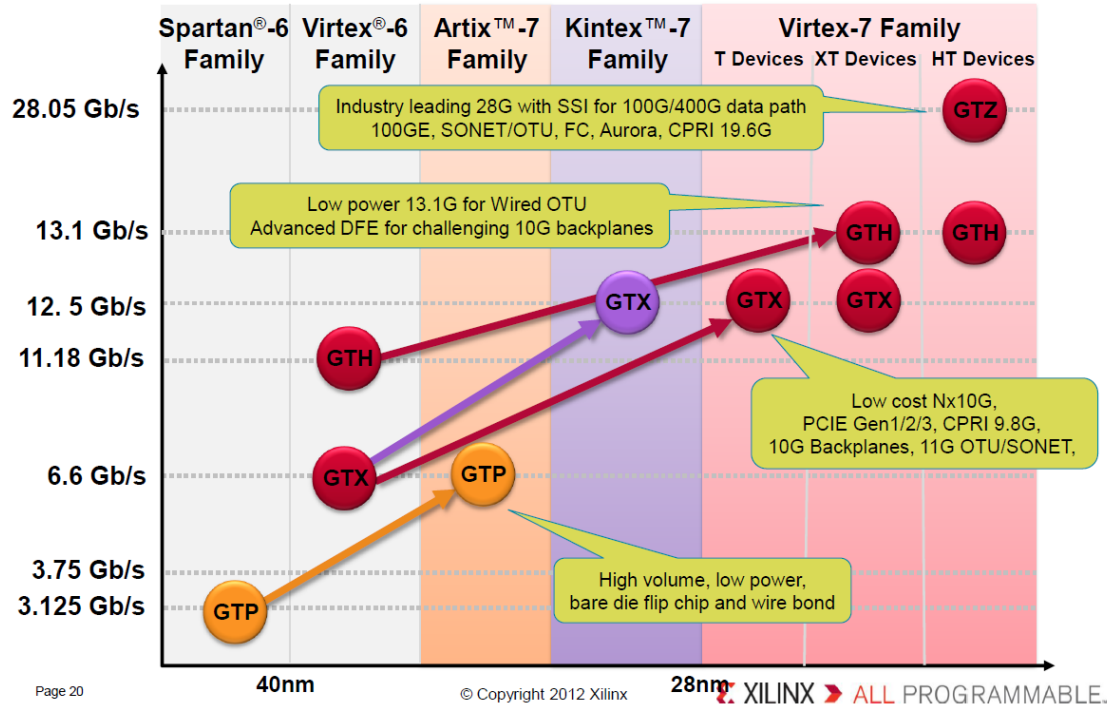
- ***A DC test, may detect these faults better than signaling tests***

An ATE on FPGA?

Massive Parallelism
- Millions of logic elements
- Thousands of 20kb memory blocks
- Thousands of DSP blocks
- Dozens of high-speed transceivers

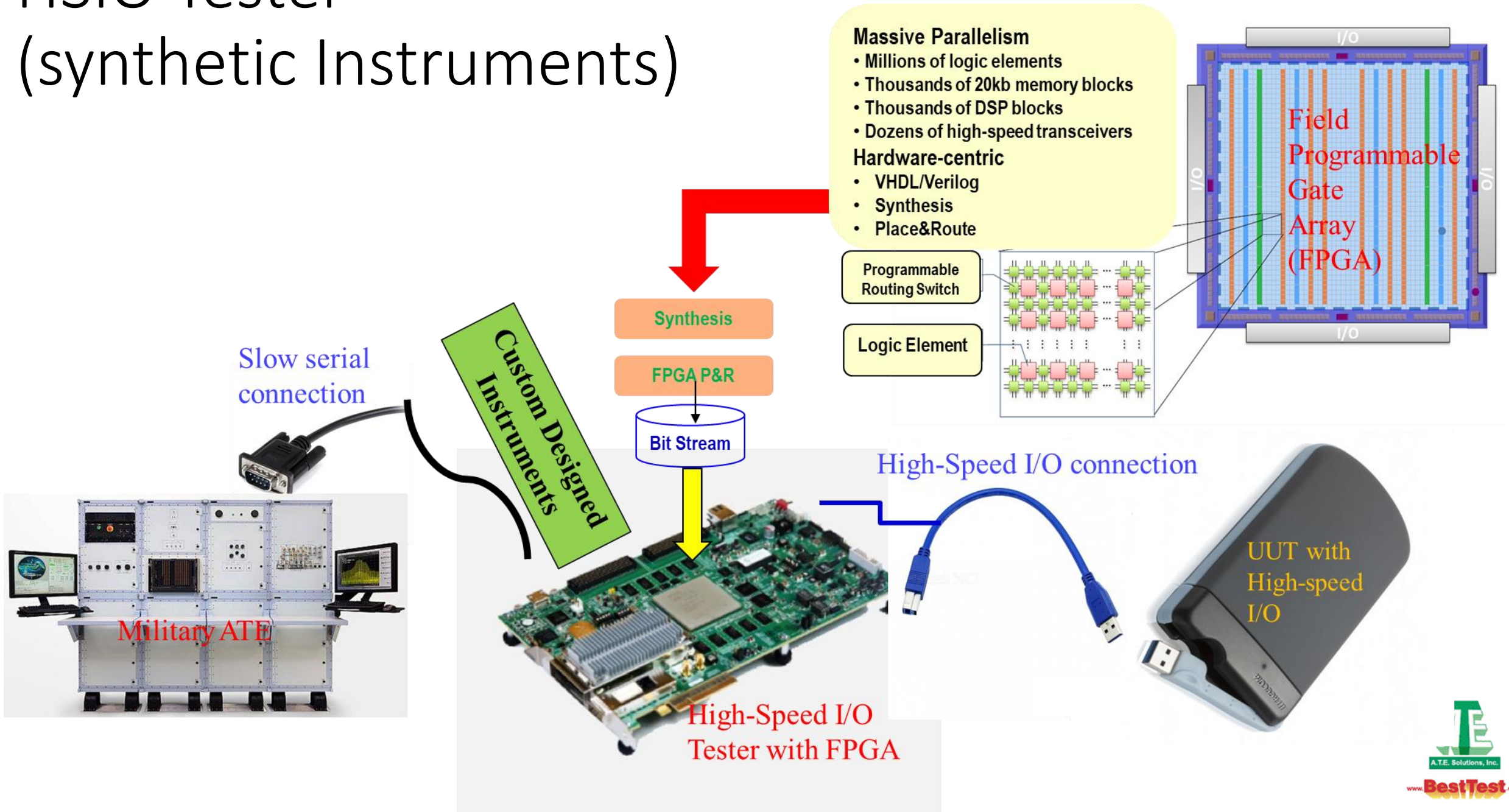
Hardware-centric
- VHDL/Verilog
- Synthesis
- Place&Route



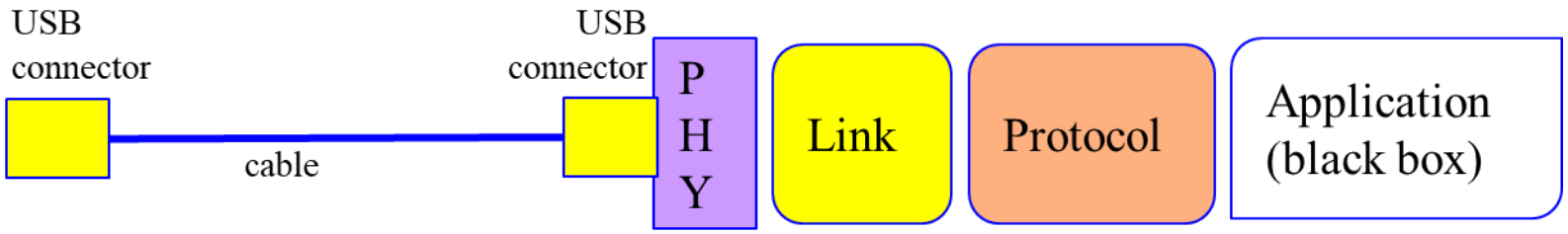


Piggyback on FPGA scaling and transceiver performance trend

HSIO Tester (synthetic Instruments)



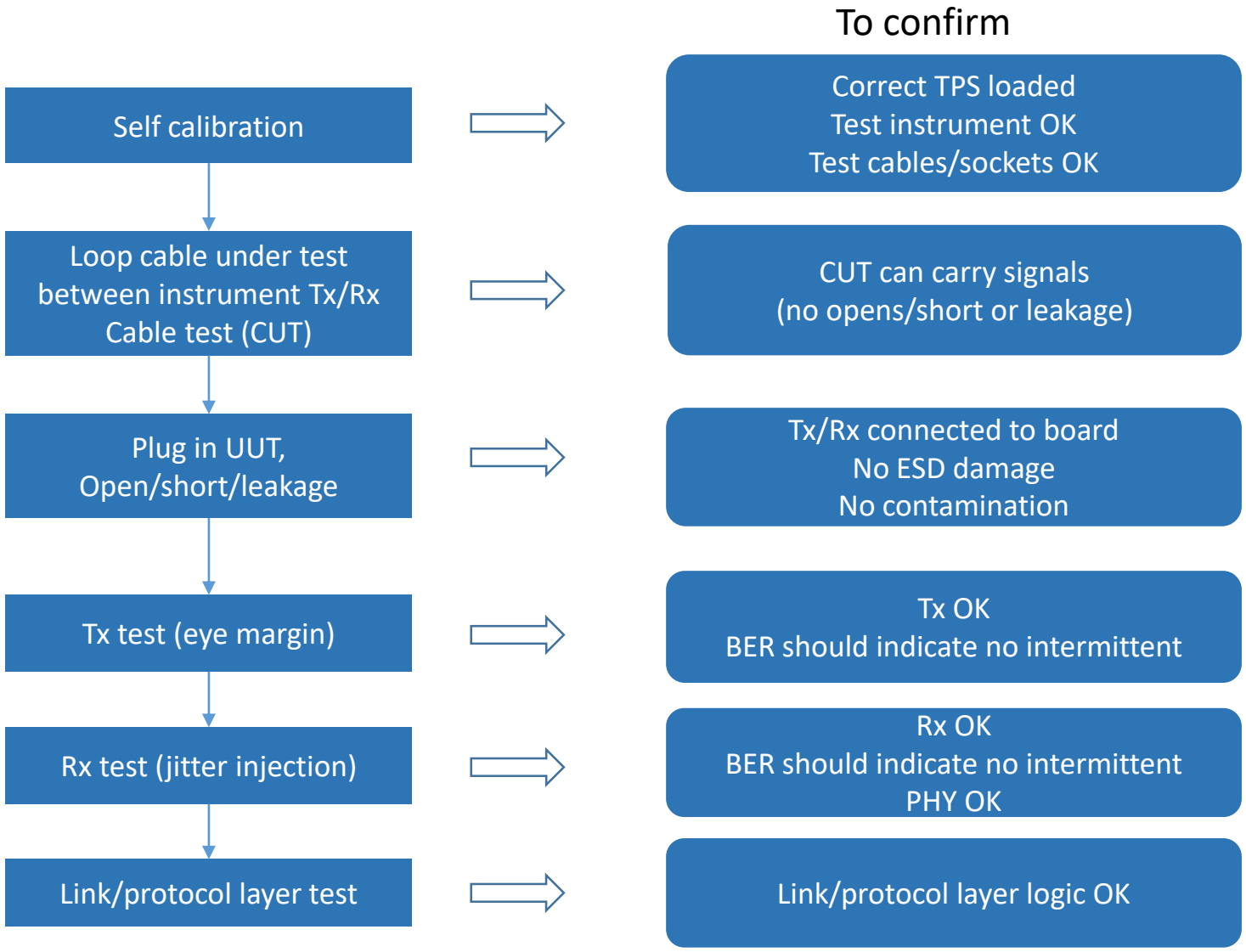
Challenges at the service depot



Which part of these is faulty?
Is it replaceable?

Diagnosing Test is critical here

Diagnosable Test Flow – incremental, progressive

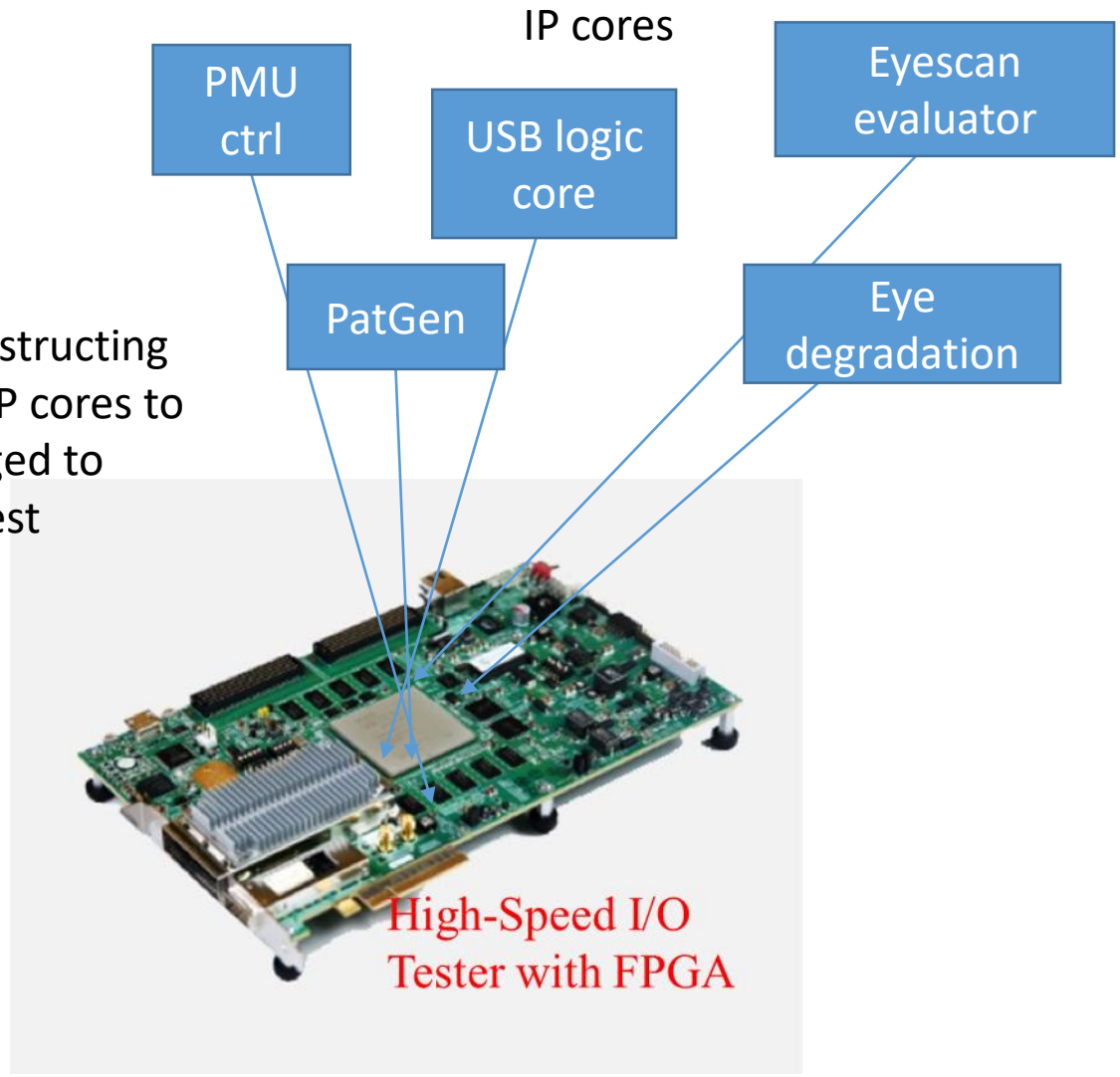


Test Methodology embedded in “firmware”

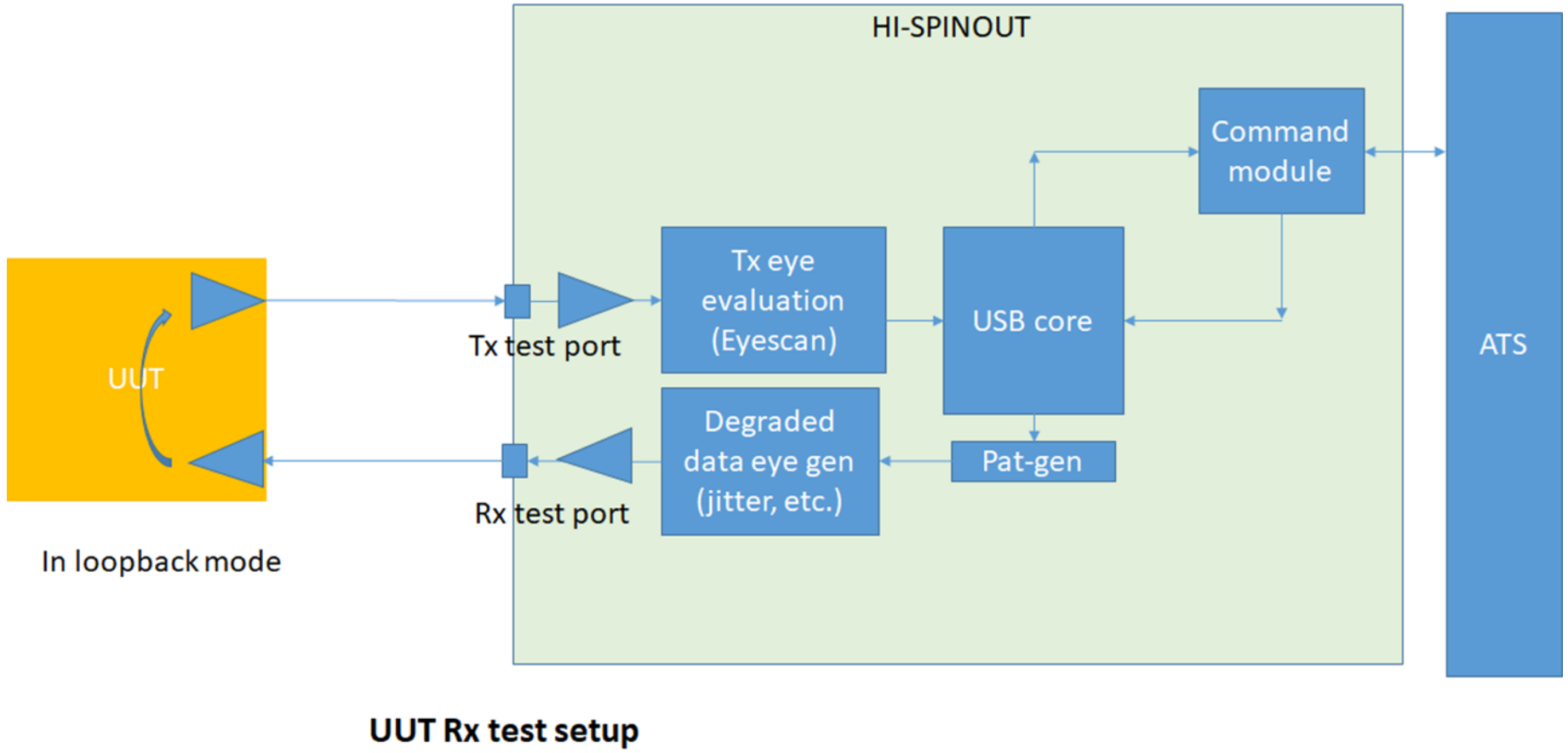
CMD -option 1, -option 2, -option n

Selftest –quick –all (default)
Cabletest –all (default) –open –leakage
Power –on –off
USB –initialize –reset –loopback
TxTest -5G (default) -2G -1G –PRBS (default) –stdeye (default) –fullresult
RxTest –PRBS (default) –jitter

These are instructing the proper IP cores to be re-arranged to perform a test



Rx sensitivity test (analog fault injection)



UUT Rx test setup

Summary

- ATE/ATS on a chip (FPGA) is possible
- Development of such a system is more cost effective and scalable
- TPS for such a system cost much less (due to simple commands and reusability) to develop

For more details, check the following posted white papers