A.T.E. Solutions, Inc.

HiSPINOUT™ PRODUCT BRIEF

High-Speed Bus Test Instrument

Key Features

- Tests high-speed data ports
- Housed in a 2U 19-inch standard chassis
- Configured as:
  - Test Instrument connected to ATE
  - PC Based Test Instrument with capability to test buses independently
- The Test Instrument configuration augments existing military and commercial ATEs with high-speed I/O bus test capabilities controlled via a serial interface
- FPGA supports up to 500 unique synthetic instrument instances and I/O speeds up to 30.5 Gbps
- Full test program for at-speed test and diagnosis of USB 3.2 Gen 1 (USB 3.0)
- Extensible to include full test of other high and low speed bus interfaces
- Provides cable pin short, pin open and current leakage tests
- Graphical User Interface used in PC Based Test Instrument simplifies system operation

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Developed under a US Navy sponsored Small Business Innovation Research (SBIR) program, the ***Hi***gh ***SP***eed ***IN***put/***OU***tput ***T***ester (HiSPINOUT) utilizes a Field Programmable Gate Array (FPGA) to deploy test instruments, called synthetic instruments (SIs). Using the FPGA's ability to reconfigure SIs in concert with A.T.E. Solutions, Inc.'s patented dynamic reconfiguration methodology, HiSPINOUT creates a bus-specific test environment. In this environment, physical (PHY) link and higher layer test sets are developed and delivered as part of the HiSPINOUT product. HiSPINOUT is normally used as an auxiliary instrument attached to an ATE to test a high-speed bus with reusable test sequences. It can also be used as a stand-alone ATE, i.e. test the bus with preprogrammed test sequences. The reusable test program reduces test program set (TPS) development effort needed to verify data bus integrity. HiSPINOUT readily interfaces with both military and commercial ATE, expanding their capabilities to test high-speed units under test (UUTs). Test developers can use simple HiSPINOUT commands to perform complex tests.

New Platform for Automated Testing

HiSPINOUT is a new approach to automate testing of electronics systems and subsystems. Traditionally, an ATE utilized general-purpose test instruments to apply and collect stimulus and response signals to a UUT. This was directed by a controller or processor responding to the scheduling by a test program set. While general-purpose instruments allowed for a wide range of stimuli and measurements, they required the test engineer to operate each instrument according to their understanding of the UUT functionality. Each resulting test program would only work on that ATE configuration and only for that UUT. Reuse of any portion of the TPS was seldom possible, requiring all TPSs to be developed essentially from scratch.

HiSPINOUT utilizes SIs and our patented *dynamic reconfiguration* embedded in FPGAs to perform more than just the functions of general-purpose instruments. SIs can also be I/O bus oriented and follow protocols required by the specific bus. Moreover, they operate and communicate at the normal operating speed of the I/O, e.g., at 5 Gbps in the case of USB 3.2 Gen 1. A set of tests

that verify the correct operation of the bus, including, but not limited to the PHY layer becomes the *reuse bus test (RBT)* delivered with HiSPINOUT or downloaded as new tests become available for other buses. The end user of HiSPINOUT can simply run the test and ensure that the UUT I/O is working properly **at-speed**. The USB 3.2 Gen 1 test, for example, will be completely reusable, saving hundreds of hours of test engineering development time.

Table 1 – HiSPINOUT Commands

Primary Test Function	Description
Self Test	Performs a self-test of HiSPINOUT.
Cable Test	Tests a connected USB cable for shorts and opens
Transmit (Tx) Test	Tests the transmit logic by setting the connected USB UUT in USB loopback mode.
Receive (Rx) Test	This test should be run after the transmit test passes. In this test jitters are added to test the Rx and its associated compensation circuits.
Link Layer Test	In this test, the USB link layer operation is validated by additional functional tests for flow control, handshaking, and error checking capabilities.
Protocol Layer Test	In this test, the USB protocol layer operation is validated. This layer is application specific.
	The following tests are specific for Mass Storage devices. Other devices may have different command sets.
Write Data Test	This test allows verification of writing specific data to the specific blocks of the mass storage.
Read Data Test	This test allows verification of reading expected data from the specific blocks of the mass storage.

As HiSPINOUT is enhanced to include other buses and I/O tests, this approach will be retained, resulting in an ATE platform fully adapted to testing any bus structure your UUT may utilize. These simple to use commands save a great deal of test engineering time and effort over manually navigating through the complex protocols using only general-purpose test instruments.

HiSPINOUT can be integrated with other testers. Communication between HiSPINOUT and other testers can be performed over standard serial ports. HiSPINOUT can be utilized as auxiliary test equipment for designated military ATE, such as the US Navy's eCASS, the US Air Force's Versatile Diagnostic Automatic Test Station (VDATS), the US Army's Integrated Family of Test Equipment (IFTE), USMC's Marine Corps Automatic Test Systems (MCATES), or virtually any ATE, including legacy ATE. HiSPINOUT can augment most ATE's capabilities to test high-speed UUTs with this same simple serial interface.

HiSPINOUT is also available as a full stand-alone system that can be used without an ATE.

Commands for Test Program Set (TPS) Developers

When HiSPINOUT is used to test a high-speed I/O bus, such as the USB 3.2 Gen 1, it runs the sequence of tests such as those detailed in Table 1. Using the commands in Table 1, the TPS developer can also customize each test by modifying test-specific operating parameters. Communication to circuitry behind the bus may be achieved using registers that can be set or read using extensions to the Write Data and Read Data commands, respectively.

An Example Test Flow for USB 3.2 Gen 1 (USB 3.0)

Figure 1 illustrates the Test Flow for the USB 3.2 Gen 1.

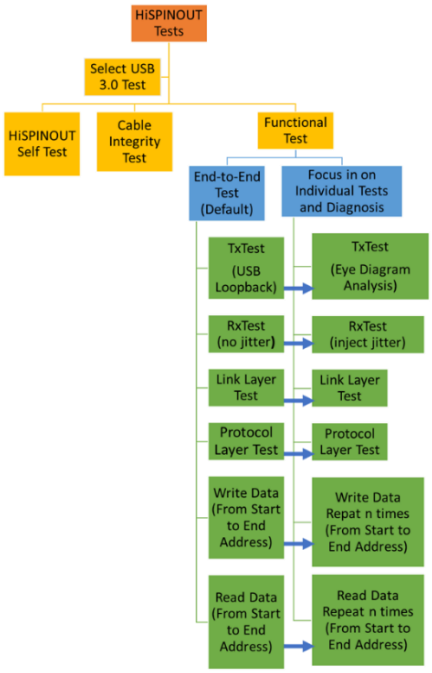
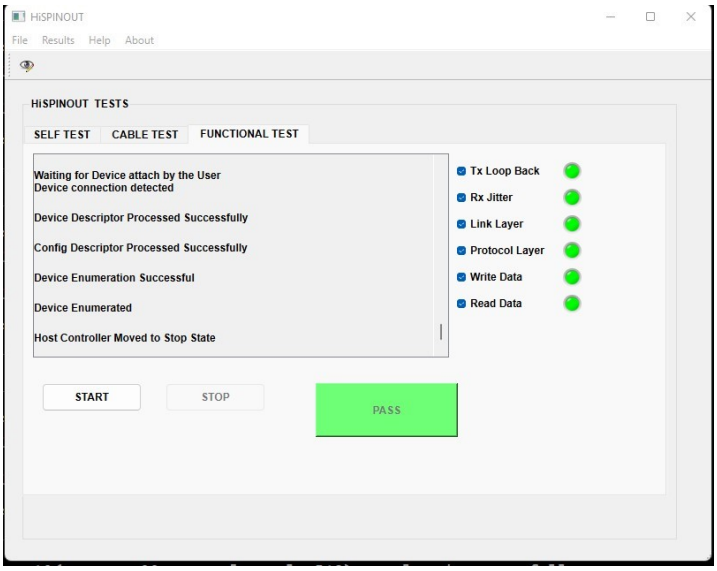


Figure 1 – HiSPINOUT Test Flow for USB 3.0

After selecting the USB 3.0 test, the user can choose to run Self-Test, Cable Integrity Test, or Functional Test. Self-Test ensures that HiSPINOUT is operating correctly. When the UUT is a cable-connected USB peripheral, then cable test is used to ensure that the UUT's cable is not defective. Finally, Functional Test is used to test the USB peripheral controller at every level of operation as well as the mission functionality accessed through the peripheral controller.

Before running any test, the test application is set in either an "Operator" or an "Expert" mode, corresponding to the End-to-End flow on the left in Figure 1, or to the Diagnosis test flow on the right in Figure 1, respectively. While both run the same tests, the difference is that an Operator will be unable to change the test operating conditions from the default values. Figure 1 illustrates the interface seen by the "Operator." The "Expert" is granted access to the operating parameters in each test step to help isolate the failure conditions.



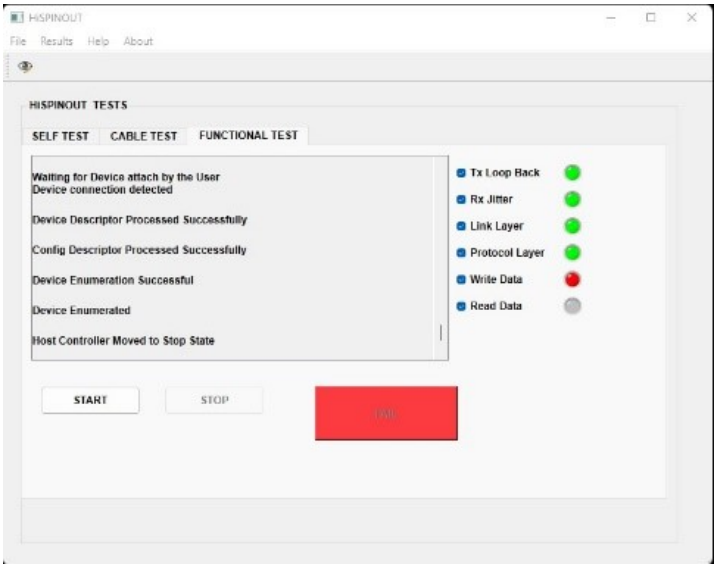


Figure 2 – Operator's Functional Test GUI. The selected tests turn on a green light for passing and a red indicator for a failing test.

When an Operator's Functional Test fails, the corresponding indicator turns red and the test stops. The operator can report only which test step failed but may not be able to determine the root cause.

When an Expert's Functional Test fails the corresponding indicator turns red and the Expert can modify the run time parameters of the test that failed, in order to isolate the root cause of the error.

An example of this is shown in Figure 4, where the Expert can modify the Rx Jitter test by adjusting the amount of jitter injected and observe the system behavior in the different scenarios.

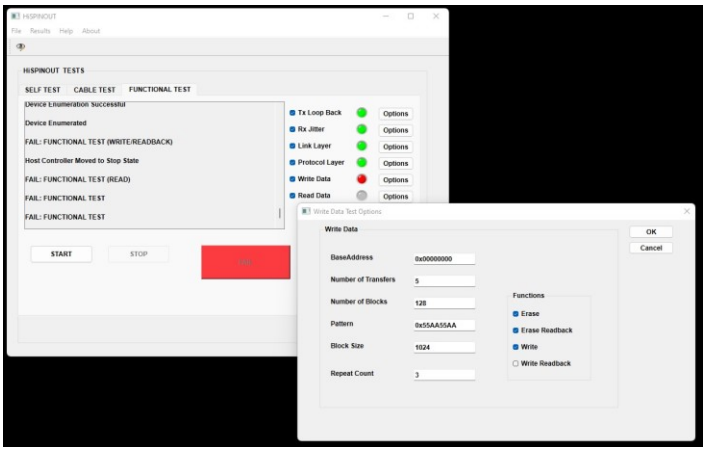


Figure 3 –Expert's Functional Test GUI. When a test fails a red light is lit and the Expert can select Options for further diagnosis.

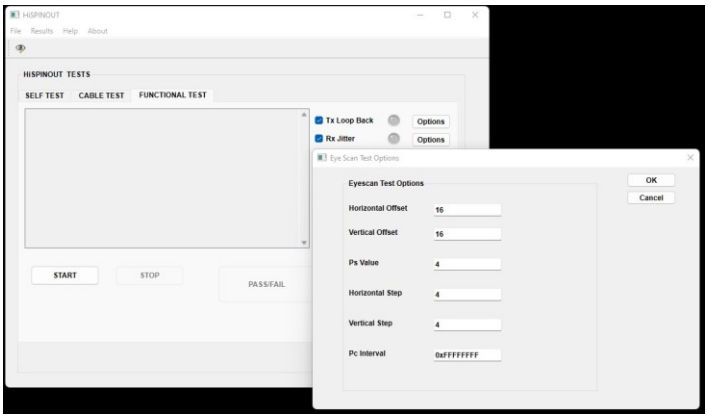


Figure 4 –Expert's Functional Test GUI allowing injection of jitter.

Figure 5 shows the normal eye diagram and one where additional jitter has been injected. The ability of the UUT's Rx to correctly receive data after jitter injection can provide information about the robustness of the UUT's Rx noise compensation circuits.

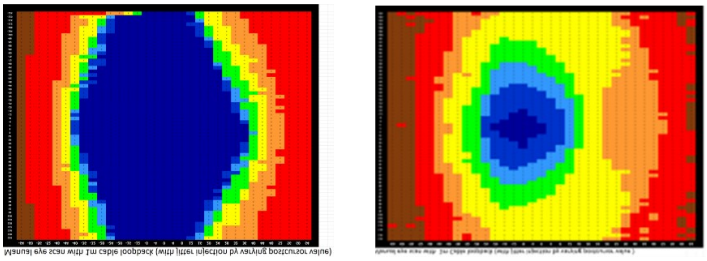


Figure 5 –A comparison of a 1 m cable before (left) and after (right) jitter injection. The Expert can input the desired amount of jitter.

Similarly, in expert mode, the Expert can adjust the type of link and protocol layer tests applied, the granularity of data collected for an eye diagram, the duration of loopback tests and other similar test parameters. All the indicated tests are delivered as part of HiSPINOUT for use with any USB 3.2 Gen 1 compliant UUT.

Specifications

HiSPINOUT	Details
Chassis	2U 19-inch rack
Chassis Dimensions	19” X 21” x 3.5”
Available Synthetic Instruments	USB 3.2 Gen 1
Maximum IO Speed	30.5 Gbps
Maximum available high-speed IOs	48
Maximum available IO pins	704
Maximum available logic	97600K system gates
Jitter Injection	Programmable using Patent Pending Technology
Total Memory	TBD with FPGA
Power Requirements	TBD watts
Operating Range	0 – 45 degrees C
Power	110V AC, 60 Hz; or 220V AC, 50 Hz
Weight	24.0 pounds
Embedded PC	**Details**
Processor Type	12th Gen Intel® Core™ i3-12100 processor
Operating System	Windows 10/11 Pro
Memory	16 GB DDR4-3200 SDRAM
Internal Storage	1TB m.2 SSD
Processor Speed	3.3 GHz
Graphics Card	Intel® UHD embedded Graphics 630
Network Interface	Integrated 10/100/1000/2500 GbE LAN
Wireless	802.11a/b/g/n/ac (1x1) Wi-Fi® and Bluetooth® 4.2 combo
Power Supply Type	500 W internal power supply
Operating Range	0 – 45 degrees C
Power	110V AC, 60 Hz; or 220V AC, 50 Hz
Weight of PC	2.0 pounds
Weight of HiSPINOUT with embedded PC	26.0 pounds

A.T.E. Solutions, Inc., established in 1984, is a highly respected test engineering and Design for Testability consulting and educational firm, providing test related products and services to industry and governments. The company is also known as Advanced Test Engineering Solutions, Inc. and as BestTest. We have a history of developing test programs for various ATEs, designing test systems, and developing test strategies. HiSPINOUT, with our patented dynamic reconfigurability, places us at the forefront of high-speed automatic I/O testing.

This brochure provides description and specification of the product at the time of printing. The most recent version of the product specification is available through www.BestTest.com/HiSPINOUT/ or upon request. For questions regarding this product, write to us at HiSPINOUT@BestTest.com.

